CLAIMS

What is Claimed is:

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1. A method of processing digital video data for displaying, said method comprising the steps of:

a) preparsing said digital video data to recover a decoding order of said digital video data;

b) decoding a variable length coding format of said digital video data;

c) moving said digital video data that has been processed by said step b); and

d) decompressing said digital video data to facilitate displaying said digital video data on an electronic display device.

2. A method as recited in Claim 1 further comprising the steps of:

accessing a first plurality of said digital video data that has been processed by said step a); and

performing said step a) on a second plurality of said digital video data while said step b) is performed on said first plurality of said digital video data.

3. A method as recited in Claim 1 further comprising the steps of:

accessing a first portion of said digital video data that has been processed by said step b) and that has been processed by said step c); and

performing said step b) on a second portion of said digital video data while said step d) is performed on said first portion of said digital video data.

4. A method as recited in Claim 1 wherein said step a) and said step d) are performed by a very long instruction word (VLIW) processor.

5. A method as recited in Claim 4 wherein said step b) is performed by a variable length decoding unit, and wherein said step a) and said step d) are performed according to time sharing criteria.

6. A method as recited in Claim 1 further comprising de-shuffling said digital video data to form a frame of said digital video data.

7. A method as recited in Claim 1 wherein said variable length coding format comprises a Huffman code format.

8. A method as recited in Claim 1 wherein said digital video data comprises DV formatted data.

9. A method as recited in Claim 1 wherein said digital video data comprises MPEG formatted data.

10. A computer-readable medium comprising computer-executable instructions for performing a method of processing digital video data for displaying, said method comprising the steps of:

a) preparsing said digital video data to recover a decoding order of said digital video data;

b) decoding a variable length coding format of said digital video data;

c) moving said digital video data that has been processed by said step b); and

d) decompressing said digital video data to facilitate displaying said digital video data on an electronic display device.

11. A computer-readable medium as recited in Claim 10 further comprising the steps of:

accessing a first plurality of said digital video data that has been processed by said step a); and

performing said step a) on a second plurality of said digital video data while said step b) is performed on said first plurality of said digital video data.

12. A computer-readable medium as recited in Claim 10 further comprising the steps of:

accessing a first portion of said digital video data that has been processed by said step b) and that has been processed by said step c); and

performing said step b) on a second portion of said digital video data while said step d) is performed on said first portion of said digital video data.

13. A computer-readable medium as recited in Claim 10 wherein said step a) and said step d) are performed by a very long instruction word (VLIW) processor.

14. A computer-readable medium as recited in Claim 13 wherein said step b) is performed by a variable length decoding unit, and wherein said step a) and said step d) are performed according to time sharing criteria..

15. A computer-readable medium as recited in Claim 10 further comprising de-shuffling said digital video data to form a frame of said digital video data.

16. A computer-readable medium as recited in Claim 10 wherein said variable length coding format comprises a Huffman code format.

17. A computer-readable medium as recited in Claim 10 wherein said digital video data comprises DV formatted data.

18. An apparatus for processing digital video data for displaying, said apparatus comprising:

a processor configured to preparse said digital video data to recover a decoding order of said digital video data; and

a variable length decoding unit coupled to said processor, wherein said variable length decoding unit is configured to decode a variable length coding format of said digital video data.

19. An apparatus as recited in Claim 18 wherein said variable length decoding unit accesses a first plurality of said digital video data that has been processed by said processor, and wherein said processor preparses a second plurality of said digital video data while said variable length decoding unit decodes said first plurality of said digital video data.

20. An apparatus as recited in Claim 18 wherein said processor is further configured to decompress said digital video data to facilitate displaying said digital video data on an electronic display device after said variable length decoding unit decodes said digital video data.

21. An apparatus as recited in Claim 20 further comprising a direct memory access (DMA) unit coupled to said processor and coupled to said variable length decoding unit, wherein said DMA unit is configured to transfer said digital video data between said processor and said variable length decoding unit, and wherein said processor accesses a first portion of said digital video data that has been processed by said variable length decoding unit, and wherein said variable length decoding unit decodes a second portion of said digital video data while said processor decompresses said first portion of said digital video data.

22. An apparatus as recited in Claim 18 wherein said processor de-shuffles said digital video data to form a frame of said digital video data after decompressing said digital video data.

23. An apparatus as recited in Claim 18 wherein said processor includes a first recovered data buffer for storing said digital video data after said processor preparses said digital video data.

24. An apparatus as recited in Claim 23 wherein said processor includes a second recovered data buffer for storing said digital video data after said processor preparses said digital video data, and wherein one of said first and second recovered data buffers is filled with said digital video data preparsed by said processor while one of said first and second recovered data buffers is emptied as said digital video data is decoded by said variable length decoding unit.

25. An apparatus as recited in Claim 18 wherein said processor includes a first decoded data buffer for storing said digital video data after said variable length decoding unit decodes said digital video data.

26. An apparatus as recited in Claim 25 wherein said processor includes a second decoded data buffer for storing said digital video data after said variable length decoding unit decodes said digital video data, and wherein one of said first and

second decoded data buffers is filled with said digital video data decoded by said variable length decoding unit while one of said first and second decoding data buffers is emptied as said digital video data is decompressed by said processor.

27. An apparatus as recited in Claim 18 wherein said processor comprises a very long instruction word (VLIW) processor.

28. An apparatus as recited in Claim 18 wherein said variable length coding format comprises a Huffman code format.

29. An apparatus as recited in Claim 18 wherein said digital video data comprises DV formatted data.

30. A digital video data decoder comprising:

a first memory buffer configured to store digital video data received from a source;

a processor coupled to said first memory buffer and configured to preparse said digital video data to recover a decoding order of said digital video data;

a variable length decoding unit coupled to said processor, wherein said variable length decoding unit is configured to decode a variable length coding format of said digital video data; and

a second memory buffer coupled to said processor and configured to store said digital video data after said digital video data is processed by said processor and said variable length decoding unit.

31. A digital video data decoder as recited in Claim 30 wherein said variable length decoding unit accesses a first plurality of said digital video data that has been processed by said processor, and wherein said processor preparses a second plurality of said digital video data while said variable length decoding unit decodes said first plurality of said digital video data.

32. A digital video data decoder as recited in Claim 30 wherein said processor is further configured to decompress said digital video data to facilitate displaying said digital video data on an electronic display device after said variable length decoding unit decodes said digital video data.

33. A digital video data decoder as recited in Claim 32 wherein said processor accesses a first portion of said digital video data that has been processed by said variable length decoding unit, and wherein said variable length decoding unit decodes a second portion of said digital video data while said processor decompresses said first portion of said digital video data.

34. A digital video data decoder as recited in Claim 30 wherein said processor de-shuffles said digital video data to form a frame of said digital video data

after decompressing said digital video data, and wherein said frame of said digital video data is stored in said second memory buffer.

35. A digital video data decoder as recited in Claim 30 wherein said processor comprises a very long instruction word (VLIW) processor.

36. A digital video data decoder as recited in Claim 30 wherein said variable length coding format comprises a Huffman code format.

37. A digital video data decoder as recited in Claim 30 wherein said digital video data comprises DV formatted data.